TSMC-99-132CC

October 15, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/623,910 07/18/03

S.L. Shue, M.H. Tsai

METHOD FOR INTEGRATING LOW-K MATERIALS IN SEMICONDUCTOR FABRICATION

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 20, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/20/03

U.S. Patent 5,827,776 to Bandyopadhyay et al., "Method of Making an Integrated Circuit which Uses an Etch Stop for Producing Staggered Interconnect Lines", discloses a multilevel interconnect structure using staggered interconnects to reduce electric field coupling between interconnect lines.

U.S. Patent 5,602,423 to Jain, "Damascene Conductors with Embedded Pillars", discloses damascene conductors with embedded pillars to prevent erosion during chemical-mechanical polishing.

U.S. Patent 5,110,712 to Kessler et al., "Incorporation of Dielectric Layers in a Semiconductor", discloses a metal interconnect in a polymer, low-K dielectric layer.

U.S. Patent 5,744,394 to Iguchi et al., "Method for Fabricating a Semiconductor Device Having Copper Layer", discloses a dual damascene process for forming inter-connections.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC18 OCT 22 2003 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-99-132CC	10/623,910
Applicant: S.L. Shue et al.	
Filing Date: 07/18/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5827776	10/27/98	Bandyopadhyay et al.	438	624	10/23/97
	5744394	4/28/98	Iguchi et al.	438	276	4/23/97
	5110712	5/5/92	Kessler et al.	430	312	4/25/90
	5602423	2/11/97	Jain	257	752	6/7/95

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant